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# Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

by H. A. Wittlinger

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. (Transconductance $g_m = \frac{\Delta i_{out}}{\Delta e_{in}}$). The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with RCA COS/MOS devices as post-amplifiers.

Fig. 1 shows the equivalent circuit for the OTA. The output signal is a "current" which is proportional to the transconductance (gm) of the OTA established by the amplifier bias current ($I_{ABC}$) and the differential input voltage. The OTA can either source or sink current at the output terminals, depending on the polarity of the input signal.

The availability of the amplifier bias current ($I_{ABC}$) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

### Circuit Description

A simplified block diagram of the OTA is shown in Fig. 2. Transistors Q1 and Q2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Fig. 3a shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a "current-mirror", with similar geometries for $Q_A$ and $Q_B$, the current I' establishes a second current I whose value is essentially equal to that of I'.

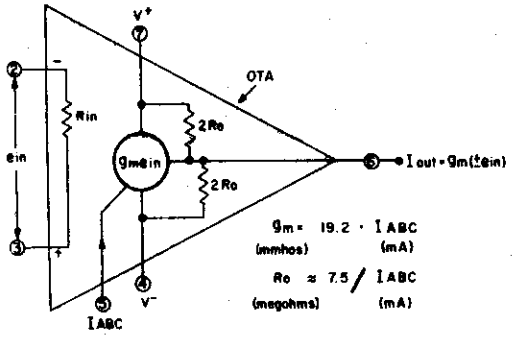



*Fig. 1— Basic equivalent circuit of the OTA.*

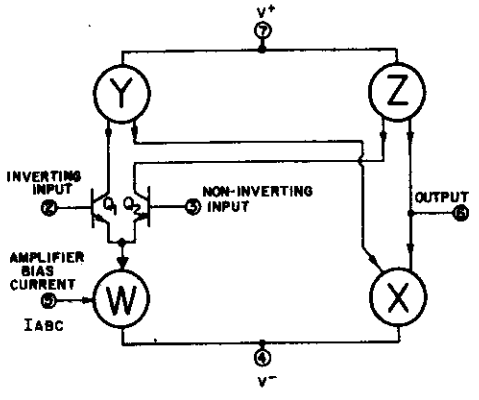



*Fig. 2— Simplified diagram of OTA.*

This basic current-mirror configuration is sensitive to the transistor beta ($\beta$). The addition of another active transistor, shown in Fig. 3b, greatly diminishes the circuit sensitivity to transistor beta ($\beta$) and increases the current-source output impedance in direct proportion to the transistor beta ($\beta$). Current-mirror W (Fig. 2) uses the configuration shown in Fig. 3a, while mirrors X, Y, and Z are basically the version shown in Fig. 3b. Mirrors Y and Z employ p-n-p transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes "current-mirrors" in more detail.

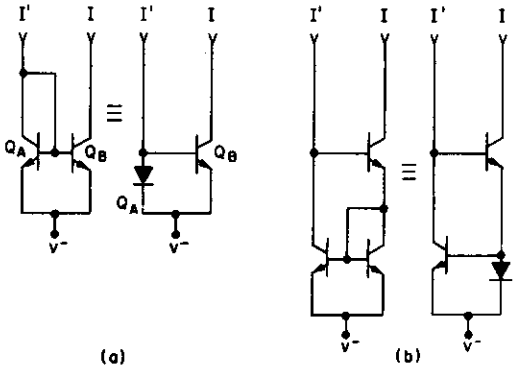



*Fig. 3— Basic types of current mirrors; a) diode-connected transistor paired with transistor; b) improved version: employs an extra transistor.*

Fig. 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, $I_{ABC}$, establishes the emitter current of the input differential amplifier Q1 and Q2. Hence, effective control of the differential transconductance ($g_m$) is achieved.

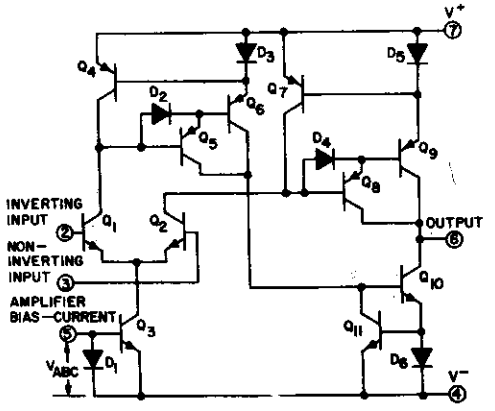



*Fig. 4— Schematic diagram of OTA types CA3080 and CA3080A.*

The $g_m$ of a differential amplifier is equal to

$$\frac{q\alpha I_C}{2KT}$$

(see Ref. 2 for derivation) where q is the charge on an electron, $\alpha$ is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), $I_C$ is the collector current of the constant-current source ($I_{ABC}$ in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_m = 19.2 \times I_{ABC}$, where gm is in mmho and $I_{ABC}$ is in milliamperes. The temperature coefficient of $g_m$ is approximately -0.33%/°C (at room temperature).

Transistor Q3 and diode D1 (shown in Fig. 4) comprise the current mirror "W" of Fig. 2. Similarly, transistors Q7, Q8 and Q9 and diode D5 of Fig. 4 comprise the generic current mirror "Z" of Fig. 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q10, Q11, and diode D6 of Fig. 2 comprise the current-mirror "X" of Fig. 2. Diodes D2 and D4 are connected across the base-emitter junctions of Q5 and Q8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the

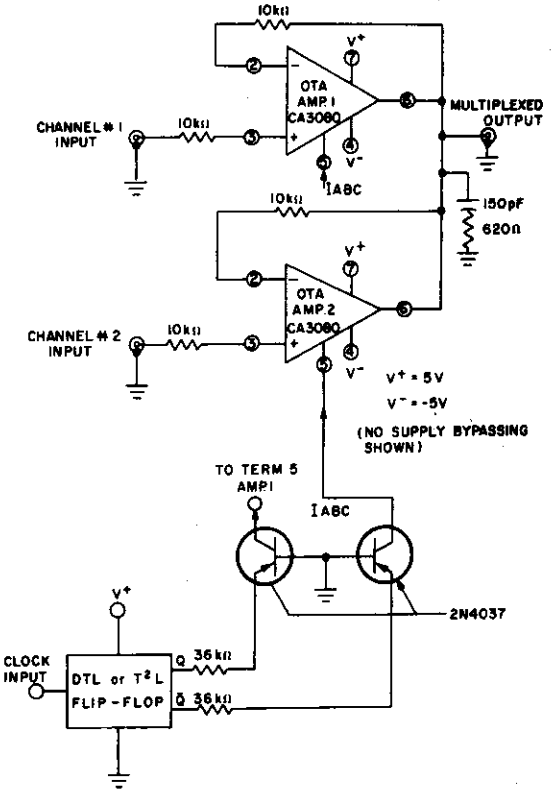



*Fig. 5— Schematic diagram of OTAs in a two-channel linear time-shared multiplex circuit.*

"Z" and "X" current-mirror of Fig. 2, providing a push-pull Class A output stage that produces full differential $g_m$. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of $g_m$ and input offset voltage, less variation of input offset voltage with variation of $I_{ABC}$ and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000 MΩ.

## APPLICATIONS

### Multiplexing

The availability of the bias current terminal, $I_{ABC}$, allows the device to be gated for multiplex applications. Fig. 5 shows a simple two-channel multiplex system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example positive and negative 5-V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15 V, with the positive-supply at 5 V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through p-n-p transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \cong 2MHz$. This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8 shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.

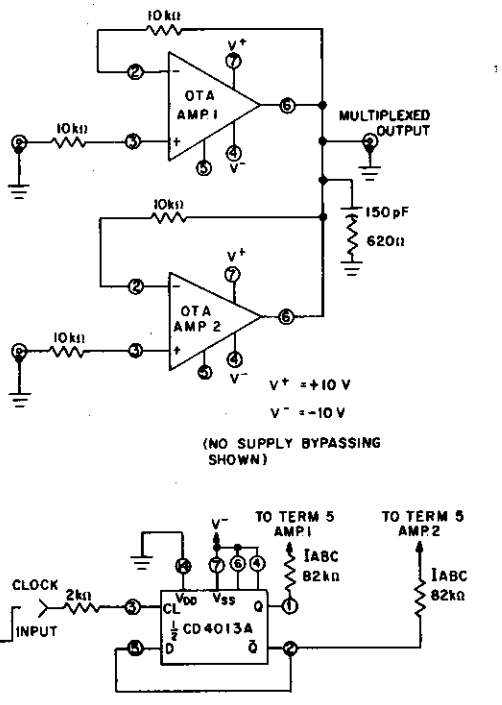
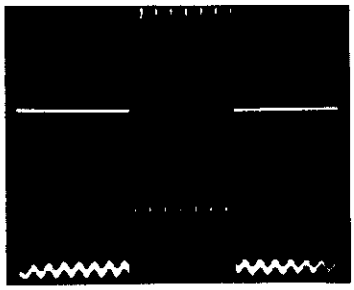



*Fig. 6— Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.*

TOP TRACE: MULTIPLEXED OUTPUT 1 V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2 V/DIV & 5 μsec/DIV

*Fig. 7— Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.*



TOP TRACE: 1 V/DIV & 100μsec/DIV — OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

*Fig. 8— Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.*

**Sample-and-Hold Circuits**

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance ($\frac{1}{g_m}$) of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_O \text{ (open-loop)}}{A \text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

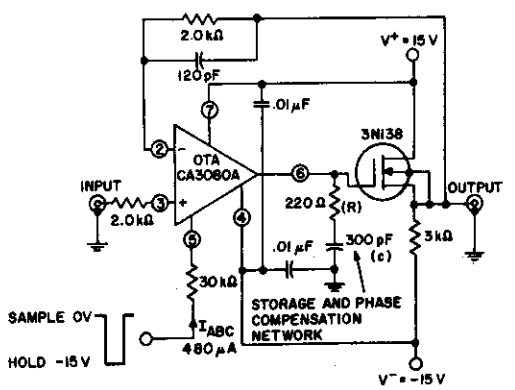



*Fig. 9– Schematic diagram of OTA in a sample-and-hold circuit.*

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA ($I = C\frac{dv}{dt}$).

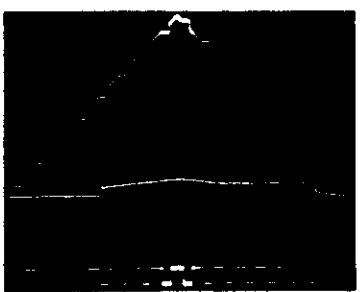



*Fig. 10– Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.*

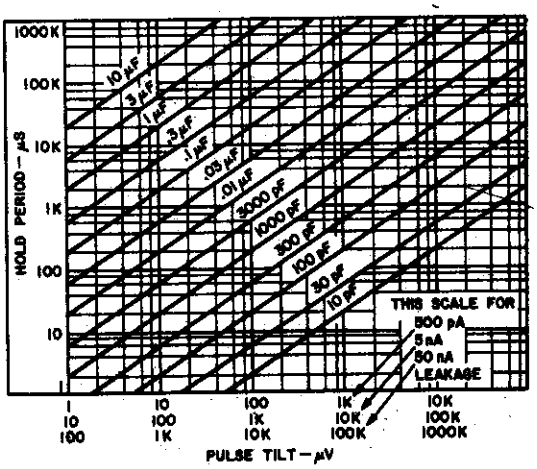
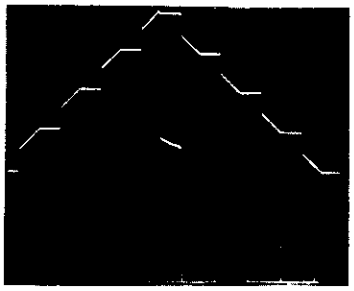


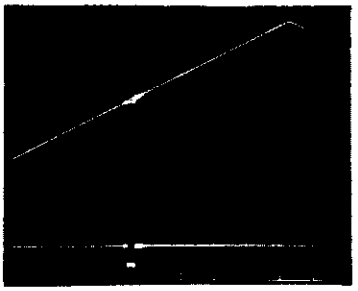

*Fig. 11– Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.*

Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.



TOP TRACE:SAMPLED SIGNAL 1 V/DIV & 20 msec/DIV
CENTER TRACE:WORSE CASE TILT 20mV/DIV & 20msec/DIV

*Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.*



TOP TRACE:INPUT AND OUTPUT SUPERIMPOSED 1V/DIV & 2μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 2μsec/DIV

*Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.*

TOP TRACE:INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100mV/DIV & 100ns/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 100 ns/DIV

*Fig. 14– Oscilloscope photo showing response of sample-and-hold circuit (Fig. 9).*

In Fig. 14, the trace of Fig. 13 has been expanded (100 mV/div and 100 ηsec/div) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1 μs. The resistor in series with the 300 pF phase-compensation capacitor was adjusted to 68 ohms for minimum recovery time.

Fig. 15 shows the basic circuit of Fig. 9 implemented with an RCA 2N4037 p-n-p transistor to minimize capacitive feedthrough. Fig. 16 shows oscilloscope photographs taken with the circuit of Fig. 15 operating in the sampling mode at supply-voltage of ±15 V. The 9.1 kΩ resistor in series with the p-n-p transistor emitter establishes amplifier-bias-current ($I_{ABC}$) conditions similar to those used in the circuit of Fig. 9.

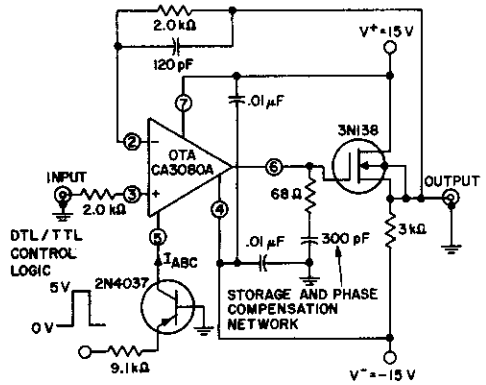
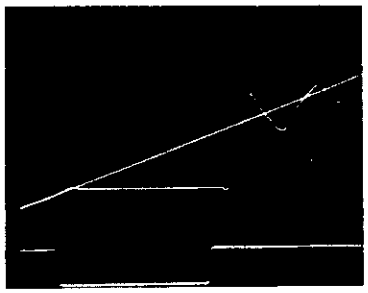



*Fig. 15– Schematic diagram of the OTA in a sample-and-hold configuration (DTL/TTL control logic).*

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$, corresponding to the first pole in the



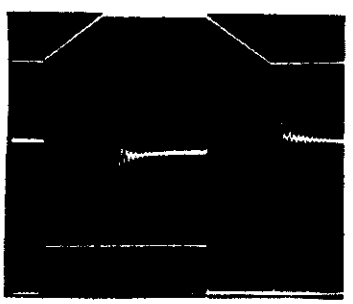
TOP TRACE:INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100 mV/DIV & 100 ns DIV
BOTTOM TRACE:SAMPLING SIGNAL 5V/DIV & 100 ns/DIV

*Fig. 16– Oscilloscope photo for circuit of Fig. 15 operating in sampling mode.*

amplifier at an output current level of 500 μA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figs. 9 and 15. The 120 pF capacitor shunting the 2 kΩ resistor improves the amplifier transient response.

Fig. 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Fig. 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dV/dt) = 1.8V/μs.

The center trace in Fig. 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2 mV/div. The output of the amplifier system settles to within 2 mV (the offset voltage specification for the CA3080A) of the input level in 1 μs after slewing.



TOP TRACE: OUTPUT 5V/DIV & 2μsec/DIV
CENTER TRACE: DIFFERENTIAL COMPARSION OF INPUT AND OUTPUT 2mV/DIV— 0 VOLTS THROUGH CENTER— 2 μsec/DIV
BOTTOM TRACE: INPUT 5V/DIV & 2μsec/DIV

*Fig. 17— Oscilloscope photo showing circuit of Fig. 9 operating in the linear sample-mode.*

Fig. 18 is a curve of slew-rate as a function of amplifier-bias-current ($I_{ABC}$) with various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current ($I_{ABC}$) when the OTA is supplying its maximum output current.

**Gain Control — Amplitude Modulation**

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current ($I_{ABC}$) in the OTA because its $g_m$ is directly proportional to the amplifier-bias-current ($I_{ABC}$). For a specified value of amplifier-bias-current, the output current ($I_O$) is equal to the product of $g_m$ and the input signal magnitude. The output voltage swing is the product of output current ($I_O$) and the load resistance ($R_L$).

Fig. 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current ($I_O$) is equal to $-g_m V_x$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, $I_{ABC}$. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current ($I_{ABC}$) through resistor Rm. Amplitude modulation of the carrier frequency occurs because variation of the voltage Vm forces a change in the amplifier-bias-current ($I_{ABC}$) supplied via resistor Rm. When Vm goes positive the bias current increases which causes a corresponding increase in the $g_m$ of the OTA. When the Vm goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the $g_m$ of the OTA.

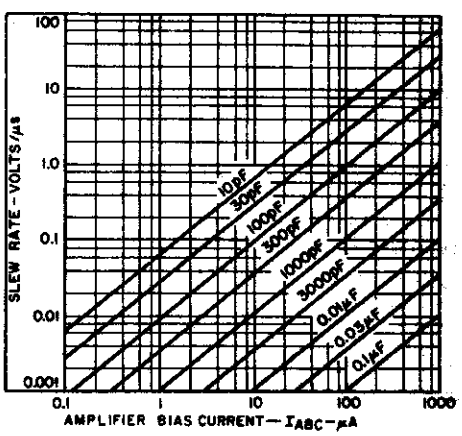



*Fig. 18— Slew rate as a function of amplifier-bias-current ($I_{ABC}$) with phase-compensation capacitance as a parameter.*

As discussed earlier, $g_m = 19.2 \times I_{ABC}$, where $g_m$ is in millimhos when $I_{ABC}$ is in milliamperes. In this case, $I_{ABC}$ is approximately equal to:

$$\frac{Vm - (V^-)}{Rm} = I_{ABC}$$

$$(I_O) = -g_m V_x$$

$$g_m V_x = (19.2)(I_{ABC})(V_x)$$

$$I_O = \frac{-19.2\,[Vm - (V^-)]\,V_x}{Rm}$$

$$I_O = \frac{19.2\,(V_x)(V^-)}{Rm} - \frac{19.2\,(V_x)(Vm)}{Rm}\ \text{(Modulation Equation).}$$

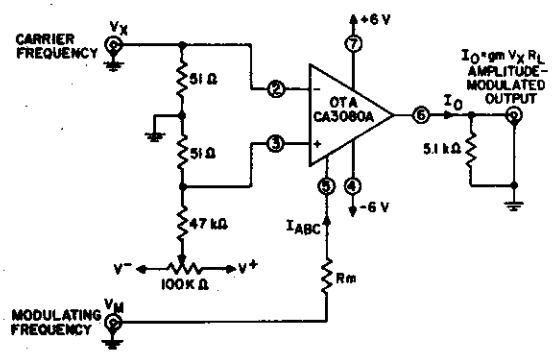



*Fig. 19– Amplitude modulator circuit using the OTA.*

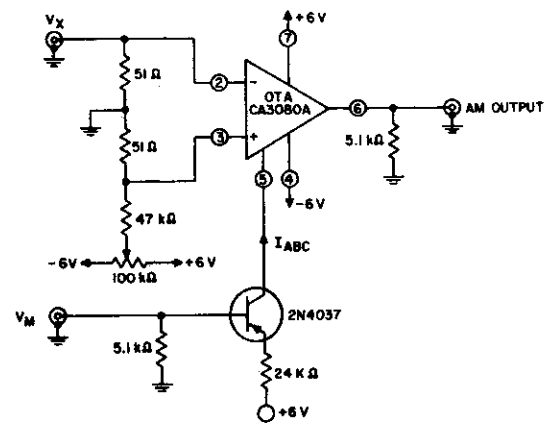



*Fig. 20– Amplitude modulator using OTA controlled by p-n-p transistor.*

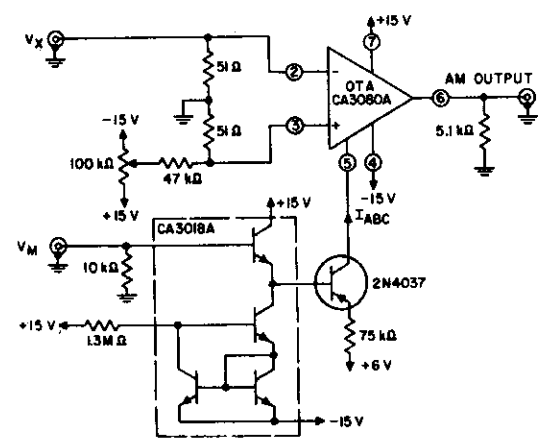



*Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.*

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of Vm, and the second term represents the modulation, which either adds to or subtracts from the first term. When Vm is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term

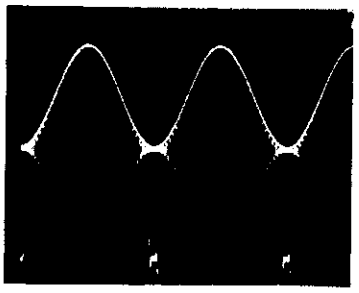
$$(19.2)\,(Vx)\ \frac{V_{ABC}}{Rm}$$

involving the amplifier-bias-current terminal voltage ($V_{ABC}$) (see Fig. 4 for $V_{ABC}$) was neglected. This term was assumed to be small because $V_{ABC}$ is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a p-n-p transistor), the effect of $V_{ABC}$ variation is eliminated and transferred to the involvement of the p-n-p transistor base-emitter junction characteristics. Fig. 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation. If an n-p-n transistor is added to the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

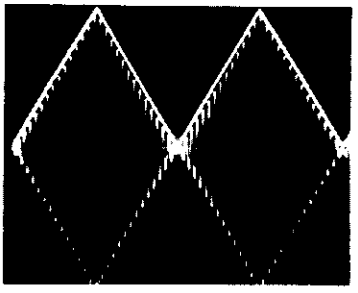
**Four-Quadrant Multipliers**

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m\,(-Vx)$ because the input is applied to the



(a) TOP TRACE: MODULATION FREQUENCY INPUT
≃ 20 VOLTS P-P & 50μsec/DIV
CENTER TRACE: AMPLITUDE MODULATE OUTPUT
500mV/DIV & 50μsec/DIV
BOTTOM TRACE: EXPANDED OUTPUT TO SHOW
DEPTH OF MODULATION 20mV/DIV
& 50μsec/DIV



(b) TOP TRACE: MODULATION FREQUENCY INPUT
20 VOLTS & 50μsec/DIV
BOTTOM TRACE: AMPLITUDE MODULATED OUTPUT
500mV/DIV & 50μsec/DIV

(c) TOP TRACE: GATED OUTPUT 1V/DIV AND 50μsec/DIV
BOTTOM TRACE: VOLTAGE EXPANSION OF ABOVE
SIGNAL—SHOWING NO RESIDUAL
1mV/DIV AND 50μsec/DIV— AT
LEAST 80 db OF ISOLATION
fq = 100 kHz

*Fig. 22— a) Oscilloscope photo of amplitude modulator circuit of Fig. 15 with $R_m$ = 40 kΩ, $V^+$ = 10 v and V- = -10 V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.*

inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when R = $1/g_m$. The current for this configuration is:

$$I_O = \frac{-19.2\ Vx\ Vm,}{Rm} \text{ and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).

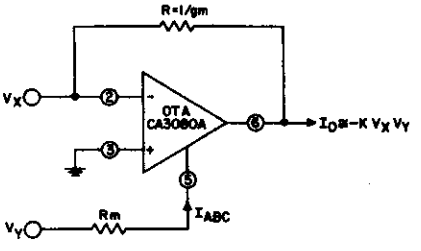



*Fig. 23— Basic four quadrant analog multiplier using an OTA.*

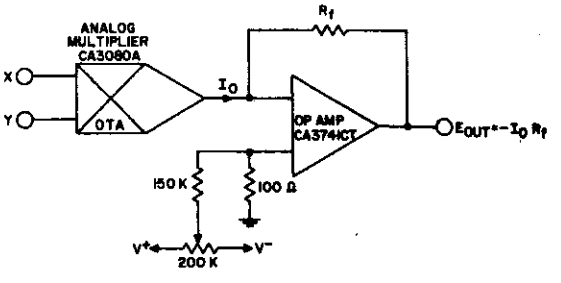



*Fig. 24— OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.*

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to

compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the $g_m$ of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.

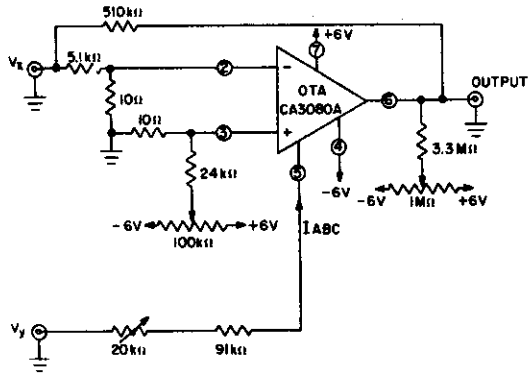



*Fig. 25– Schematic diagram of analog multiplier using OTA.*

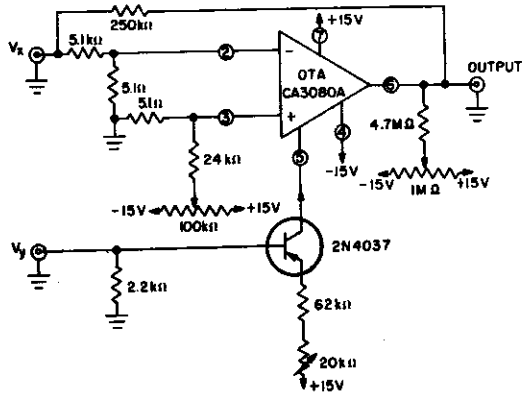
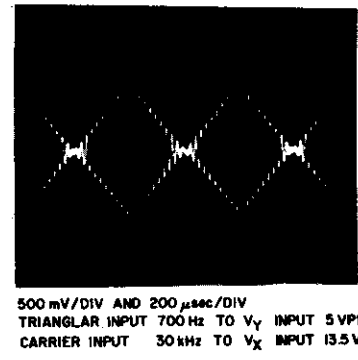
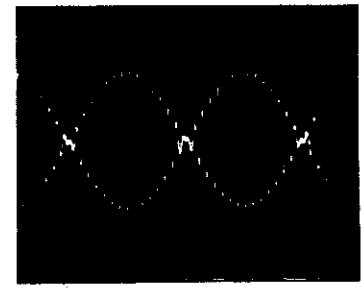
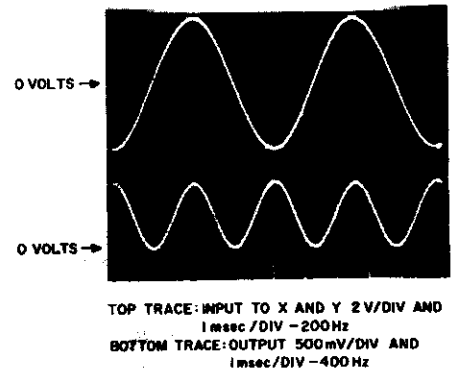



*Fig. 26– Schematic diagram of analog multiplier using OTA controlled by a p-n-p transistor.*




(a)




(b)

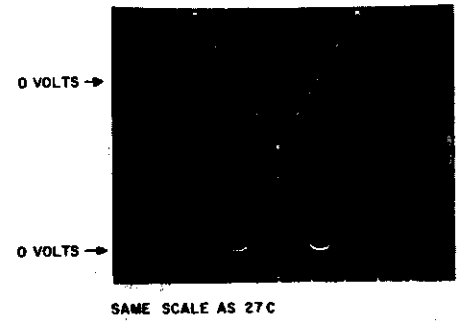



*Fig. 27– a) Waveforms observed with OTA analog multiplier used as a suppressed carrier generator; b) waveforms observed with OTA analog multiplier used in signal-squaring circuits.*

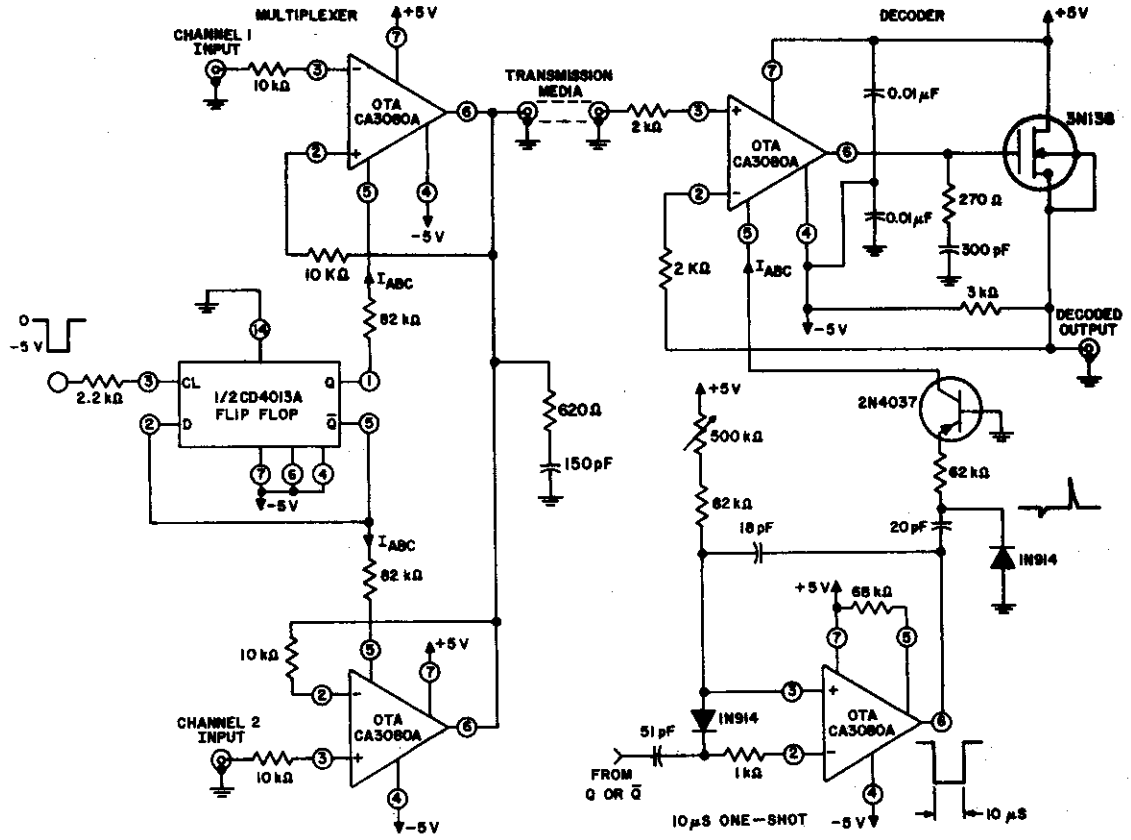



*Fig. 28– Two-channel multiplexer and decoder using OTAs.*

2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the $g_m$ balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the $g_m$ of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the $V_{be}$ temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

Figs. 27a and 27b show oscilloscope photographs of the output signals delivered by the circuit of Fig. 26 which is connected as a suppressed-carrier generator. Figs. 27c and 27d contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular-wave inputs.

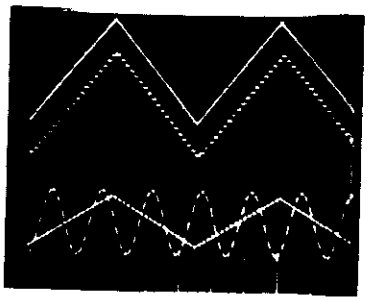
If ±15-V power supplies are used (shown in Fig. 26), both inputs can accept ±10-V input signals. Adjustment of this multiplier circuit is similar to that already described above.

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

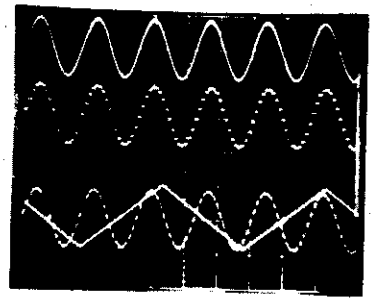
Other forms of four-quadrant multipliers using operational transconductance amplifiers have been published. (See Ref. 2.) the circuit shown in Ref. 2 tends to reduce the effects of the previously discussed $g_m$ temperature dependency.

**Linear Multiplexer – Decoder**

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Fig. 28. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Fig. 29 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10 μsec delay- "one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-

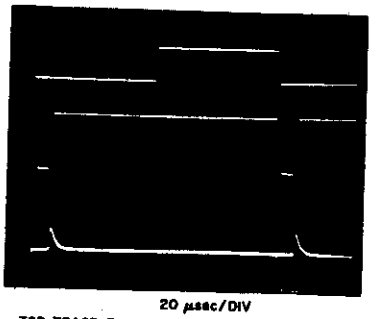


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (2 VOLTS/DIV)

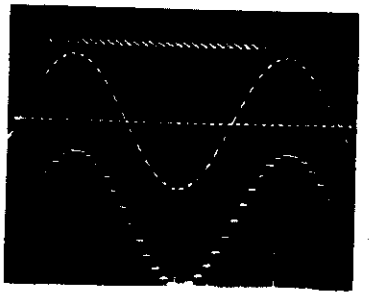


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (1 VOLT/DIV)

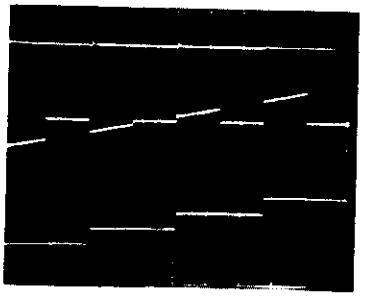
*Fig. 29– Waveforms showing operation of linear multiplexer/sample-and-hold decode circuitry (Fig. 28).*



(a) 20 μsec/DIV
TOP TRACE: FLIP-FLOP OUTPUT (5 VOLTS/DIV)
CENTER TRACE: "ONE-SHOT" OUTPUT (5 VOLTS/DIV)
BOTTOM TRACE: PULSE AT THE COLLECTOR OF THE 2N4037 TRANSISTOR (0.1 VOLTS/DIV)



(b) TOP TRACE: COLLECTOR OF PNP TRANSISTOR (0.5 V/DIV)
CENTER TRACE: MULTIPLEXED OUTPUT WITH ONE CHANNEL INPUT GROUND (0.5V/DIV)
LOWER TRACE: DECODED OUTPUT (0.5 V/DIV)
TIME ALL SCALES: 5 msec/DIV



(c) TIME EXPANSION TO 500 μsec/DIV

*Fig. 30– (a) Waveforms showing timing of flip-flop, delay– "one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). (c) 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).*

hold circuit for approximately 1 μs. Fig. 30 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10 μsec "one-shot" to decode a signal.

**High-Gain, High-Current Output Stages**

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOS/FET) shown in Fig. 9. This configuration yields a voltage gain equal to the ($g_m$) ($R_o$) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Fig. 9) are limited by the 3N138 MOS/FET performance and its source-terminal load. In the positive direction, the MOS/FET may be driven into saturation; the source-load resistance and the MOS/FET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CD4007A (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CD4007A has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/μsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/μsec (shown in Fig. 32). Even when the three "inverter"/amplifiers in the CD4007A are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/μsec. A slew-rate of about 1 V/μsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

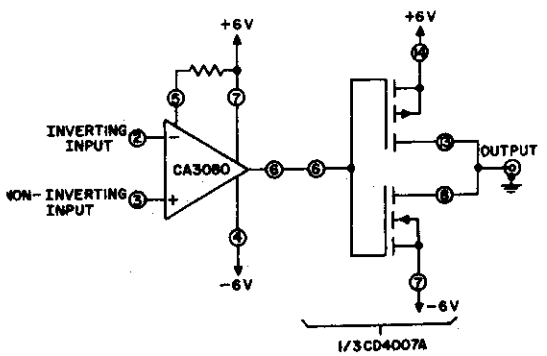



*Fig. 31– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.*

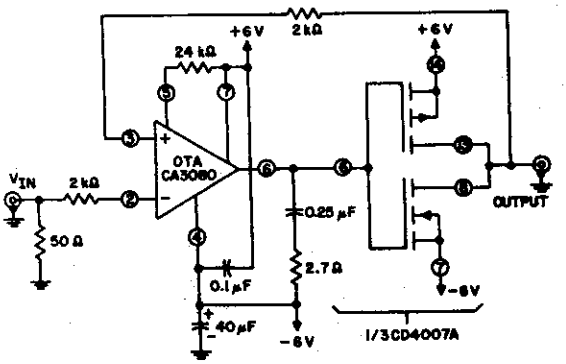



*Fig. 32– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.*

**Precision Multistable Circuits**

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

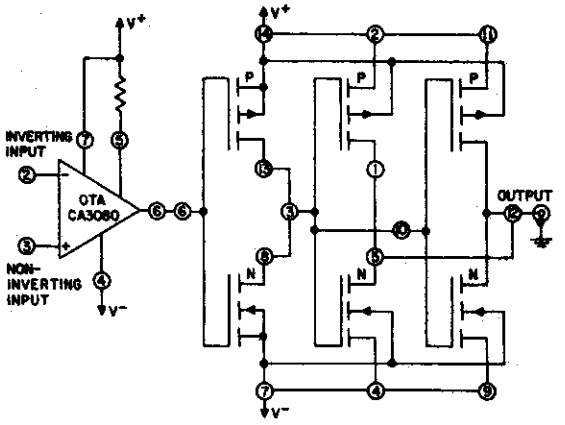



*Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.*

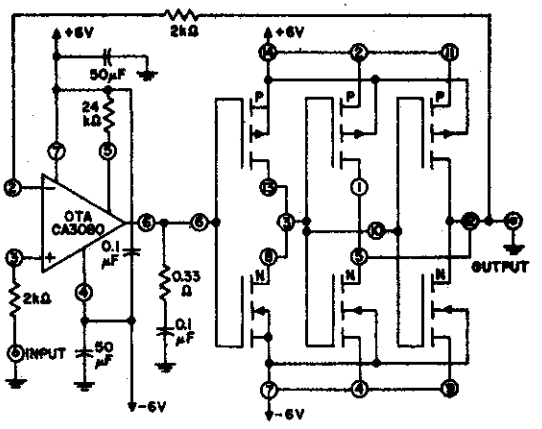
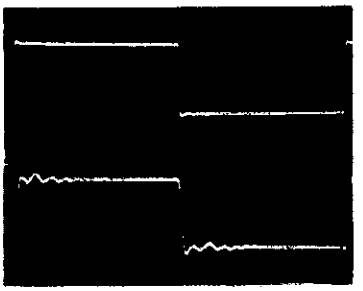



*Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).*

(a)

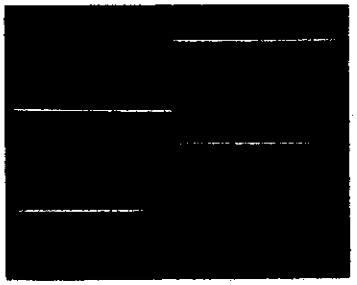
TOP TRACE: INPUT-5 V/DIV-100 μsec/DIV
BOTTOM TRACE: OUTPUT SAME SCALE

(b)



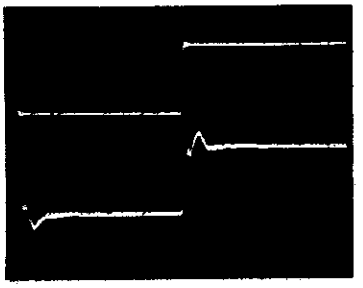
TOP TRACE:INPUT-50 mV/DIV-1 μsec/DIV
BOTTOM TRACE:OUTPUT-SAME SCALE

(c)



TOP TRACE:INPUT-5 V/DIV-100 μsec/DIV
BOTTOM TRACE:OUTPUT-SAME SCALE

(d)



TOP TRACE:INPUT-50 mV/DIV-1 μsec/DIV
BOTTOM TRACE:OUTPUT-SAME SCALE

*Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.*

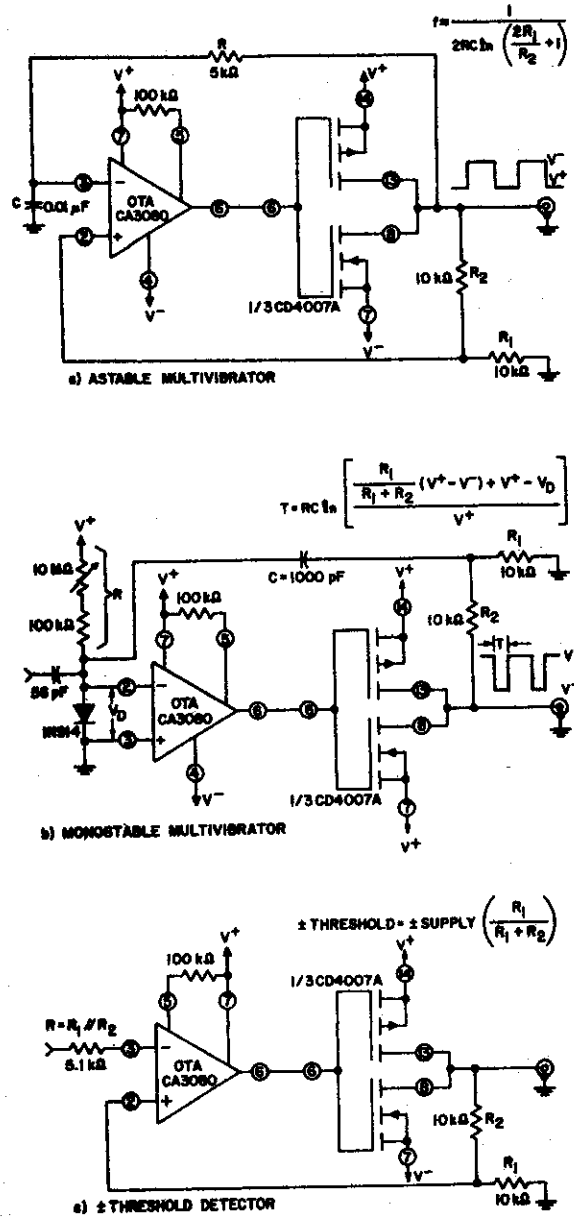



*Fig. 36– Multistable circuits using the OTA and COS/MOS Inverter/Amplifiers: a) astable multivibrator; b) monostable multivibrator; c) threshold detector (plus or minus). For greater current output, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown.*

Fig. 36 shows a variety of circuits that can be assembled using the CA3080 to drive one "inverter"/amplifier in the CD4007A. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs. power consumption tradeoffs may be made by adjustment of the $I_{ABC}$ current to the CA3080. The quiescent power consumption of the circuits shown in Fig. 36 is typically 6 mW, but can be made to operate in the micropower region by suitable circuit modifications.

### Micropower Comparator

The schematic diagram of a micropower comparator is shown in Fig. 37. Quiescent power consumption of this circuit is about 10 μW (typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420 μW. Under these conditions, the circuit responds to a differential input signal in about 8 μsec. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 nsec., but the power consumption rises to 21 mW.

The differential amplifier input common-mode range for the circuit of Fig. 37 is -1V to +10.5 V. Voltage of the micropower comparator is typically 130 dB. For example, a 5 μV input signal will toggle the output.

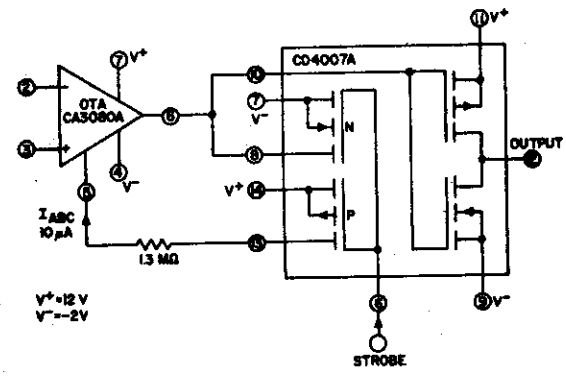



*Fig. 37– Schematic diagram of micropower comparator using the CA3080A and COS/MOS CD4007A.*

## APPENDIX I
## CURRENT MIRRORS

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Fig. A shows this basic configuration of the current-mirror. Q2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_b$. If a current $I_1$ is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q2 such that Q2 "sinks" the applied current $I_1$.

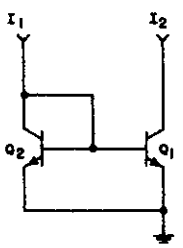



*Fig. A— Diode – transistor current source.*

If the base of a second transistor (Q1) is connected to the base-to-collector junction of Q2, shown in Fig. A, Q1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current ($I_1$) and the collector current ($I_2$) of transistor Q, is due to the fact that the base-current for both transistors is supplied from $I_1$. Fig. B shows this current division, using a unit of base current (1) to each transistor base. This base

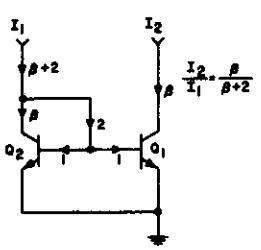



*Fig. B— Diode – transistor current source. Analysis of current flow.*

current causes a collector current to flow in direct proportion to the $\beta$ of each transistor. The ratio of the "sinking" current $I_2$ to the input current $I_1$ is therefore equal to $\frac{I_2}{I_1} = \beta/(\beta+2)$. Thus, as $\beta$ increases, the output "sinking" current ($I_2$) level approaches that of the input current ($I_1$). The curves in Fig. C show this ratio as a function of the transistor $\beta$. When the transistor $\beta$ is equal to 100, for example, the difference between the two currents is only two percent.

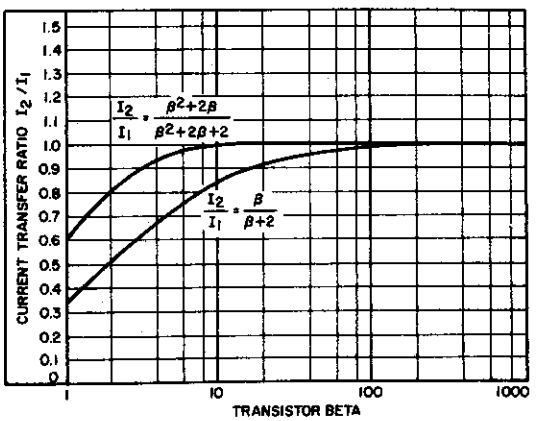



*Fig. C— Current transfer ratio $I_2/I_1$ as a function of transistor beta.*

Fig. D shows a curve-tracer photograph of characteristics for the circuit of Figs. A and B. No consideration in this discussion is given to the variation of the transistor (Q1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q1.


*Fig. D— Photo showing results of Figs. A & B.*

This diode-connected transistor (Q3 in Fig. E) may be considered as a current-sampling diode that senses the emitter-current of Q1 and adjusts the base current Q1 (via Q2) to maintain a constant-current in $I_2$. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Fig. F shows the improved output resistance characteristics of the circuit of Fig. E. (Compare Fig. D and F).

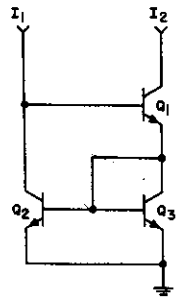



*Fig. E– Diode – 2 transistor current source.*

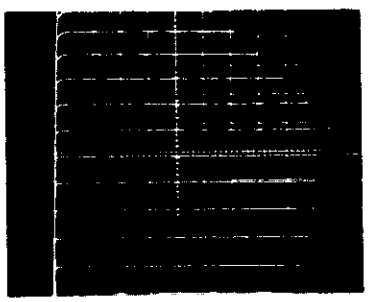



*Fig. F– Photo showing results of Fig. E.*

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3.

The resulting current-transfer ratio $I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$. Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio ($I_2/I_1$) is improved by the $\beta^2$ term, and reduces the significance of the $2\beta + 2$ term in the denominator.

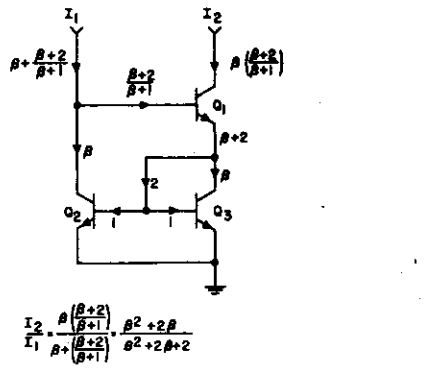



*Fig. G– Current flow analysis of Fig. E.*

## Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

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## References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.
2 RCA published data for CA3060 File No. 404